[0018] FIG. 3 illustrates a crack forming in a conventional flip-chip structure after mounting on a printed circuit board substrate and thermal cycling;

[0019] FIGS. 4A-B illustrate a solder bump structure according to an embodiment detailed in U.S. Patent Application No. 10/339,456;

[0020] FIGS. 5A-B illustrate a solder bump structure according to an exemplary embodiment of the present invention;

[0021] FIGS. 6A-D illustrate a solder bump structure according to another exemplary embodiment of the present invention;

[0022] FIGS. 7A-C illustrate a solder bump structure according to yet another exemplary embodiment of the present invention;

[0023] FIGS. 8A-E illustrate a solder bump structure according to another exemplary embodiment of the present invention;

[0024] FIGS. 9A-B illustrate a solder bump structure according to another exemplary embodiment of the present invention;

[0025] FIGS. 10A-J are cross-sectional views illustrating an exemplary embodiment of a manufacturing process for producing a solder bump structure according to an exemplary embodiment of the present invention;

[0026] FIGS. 11A-E are cross-sectional views illustrating an exemplary embodiment of a manufacturing process for producing a solder bump structure according to an exemplary embodiment of the present invention;

[0027] FIGS. 12A-B are cross-sectional views illustrating an exemplary mounting/reflow process for producing a semiconductor device utilizing an exemplary embodiment of the present invention; and

[0028] FIG. 13A-E are plan views illustrating various protrusion configurations.

[0029] These drawings have been provided to assist in the understanding of the exemplary embodiments of the invention as described in more detail below and should not be construed as unduly limiting the invention. In particular, the relative spacing, sizing and dimensions of the various elements illustrated in the drawing are not drawn to scale and may have been exaggerated, reduced or otherwise modified for the purpose of improved clarity. Those of ordinary skill in the art will also appreciate that certain layers that may be commonly utilized in the manufacture of semiconductor devices including, for example, photoresist patterns and multilayer metallization structures, have been omitted simply to improve clarity and reduce the number of drawings.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0030] The present invention is at least partially characterized by the inclusion of one or more reinforcing protrusions within the solder bump material to suppress the formation and/or propagation of cracks within the solder bump material during the operation of the final device, due at least in part to thermal cycling and mechanical stresses induced by mismatched coefficients of expansion between the various components. While the reinforcing protrusions can take any number of forms, the invention will be described below with reference to several exemplary embodiments.

[0031] FIG. 4A is a cross-sectional view of a solder bump structure according to an embodiment of an invention disclosed in U.S. Patent Application No. 10/339,456, and FIG. 4B provides a cross-sectional view along the line I-I' of FIG. 4A. The solder bump structure includes a contact pad 2 of an electronic device such as a semiconductor chip 1 intended for use in a flip chip package or a wafer level package. An opening is defined in